## Remarks

Claims 6, 14, 24 and 29 are amended. No claims are added or cancelled. Claims 1 – 29 are pending. Reexamination and reconsideration of this application, as amended, are respectfully requested.

The Examiner rejected each of claims 1 – 29 as being made obvious in view of a combination of references including at least U.S. Patent No. 6,073,253 to Nordstrom et al. (the "'253 patent") and U.S. Patent No. 6,212,587 (the "'587 patent") under 35 USC § 103(a). This rejection is respectfully traversed.

The specification of the present application relates to, among other things, a peripheral device coupled to a data bus which defines a plurality of "device functions." The device functions are accessible through a single interface coupling the peripheral device to the data bus. A first processing system coupled to the data bus may address bus transactions to a first of the device functions and a second processing system coupled to the data bus may address bus transactions to a second of the device functions. [Specification, para. 24] Accordingly, the first and second processing systems may each access different device functions defined by a single peripheral device.

A prima facie case of obviousness under 35 U.S.C. § 103(a) first requires that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined)

must teach or suggest all the claim limitations. . . The teaching or suggestion to make the claimed combination and the ***reasonable expectation of success*** must both be found in the prior art, not in applicant's disclosure. [emphasis added] *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8th Edition, August 2001, § 2143.

Regarding a potential motivation or suggestion to combine the '253 and '587 patents, the Examiner merely makes reference to the '587 patent at col. 2, ll. 33 – 35 which provides:

> In order to incorporate $I_2O$ technology in a computer system and realize the benefits afforded by the $I_2O$ technology, operating systems need to differentiate between ***peripheral devices*** which are under the control of a $I_2O$ input/output processor (IOP) and peripheral devices which are not. [emphasis added]

While this excerpt may suggest or motivate the solution described in the '587 patent (i.e., having a device proxy agent 280 to control access to individually hidden "peripheral devices"), this does not appear in any way to suggest or motivate the incorporation of a multi-function device as shown in the '253 patent. If anything, by specifically identifying the "need to differentiate between ***peripheral devices***," '587 patent "teaches away" from the notion of allocating control of functions within a device between an IOP and other entities (i.e., differentiating among multiple device functions of a peripheral device). Accordingly, the applicant respectfully submits that there is no suggestion or motivation to combine the '587 and '253 patents.

The '587 patent appears to describe the use of a device proxy agent 280 for controlling access to devices 270 on a PCI bus 230 which are to be hidden from CPUs 250. Devices on the PCI bus 230 are to be accessed using memory space decoding

and an I/O processor (IOP) 290 controls all access to the devices 270. Addressing memory space for communicating with the devices 270 is initially assigned to the device proxy agent 280 rather than to the devices 270. The IOP 290 stores information pertaining to the hidden devices 270 in the assigned memory space while the host CPUs 250 do not "see" the hidden devices 270 and do not attempt to communicate with them directly.

While the '587 patent appears to show how devices 270 may be hidden from memory addressing by the host CPUs 250, the '587 patent does not appear to show how the CPUs 250 are capable of configuring an individual function of a device on the PCI bus 230 while another function of the device is being hidden from the CPUs 250. Figures 14A through 14C of the '587 patent show how a standard system BIOS routine (presumably executed by the CPUs 250) initiates a configuration write transaction to the IOP 290. The IOP 290 may then take action to hide the devices 270 from subsequent configuration transactions initiated by the standard system BIOS routine. However, there is no indication of how this configuration process may be applied to a multifunction device 260 shown in Figure 2B of the '253 patent individual device. It is not shown in either the '587 or '253 patent how the IOP 290 may conceal at least one device function of the device 260 from the standard system BIOS routine and not the other using the process illustrated in Figures 14A through 14C of the '587 patent. Accordingly, the applicant respectfully submits that there would have been no reasonable expectation of success in combining the '587 and '253 patents to provide the claimed combinations.

The Examiner also rejected claim 6 as being made obvious by the '587 and '253 patents further in view of U.S. Patent No. 6,647,434 (the "'434 patent") under 35 U.S.C. § 103(a). This rejection is respectfully traversed.

The specification of the present application relates to, among other things, an I/O processor 14 that initiates a first bus transaction at block 102 to configure a first device function of a peripheral device 16 and a second bus transaction at block 104 to configure a second device function of the peripheral device 16. The I/O processor 14 initiates a third bus transaction at block 106 to conceal the first device function from any subsequent enumeration transactions (e.g., initiated by the host system 12). However, the I/O processor 14 may continue to communicate with the first device function (while the first device function is being "hidden" from the host system 12). [Specification, paras. 26 – 27]

The '434 patent appears to describe a method of disabling individual functions of a PCI device by setting individual bits in a register byte 305 of a configuration register (Figure 3). Accordingly, control logic 207 (Figure 2) may write configuration information to enable or disable individual functions of the PCI device. Once a function is disabled, no process apparently communicates with the disabled function.

In addition to distinguishing over the combination of the 587 and '253 patents (as pointed out by the Examiner), claim 6 distinguishes over the '434 patent by reciting, among other things:

> logic to set information in a configuration header maintained at the peripheral device to conceal the first device function from the second processing system ***while enabling the first processing system to communicate with the first device function*** [emphasis added]

By merely showing how a function of a peripheral device may be disabled, the '434 patent does not disclose, suggest or make obvious "enabling the first processing system to communicate with the [concealed] first device function" as recited in claim 6. Accordingly, the applicant respectfully submits that claim 6 distinguishes over the combination of the '587, '253 and '434 patents. While differring from the scope of claim 6 at least in part, claims 14, 24 and 29 recite limitations similar to those in claim 6 which are quoted above. Accordingly, the applicant respectfully submits that these claims similarly distinguish over the combination of the '587, '253 and '434 patents.

The applicants respectfully submit that the application is now in form for allowance. Reconsideration of this case is respectfully requested. Please charge Deposit Account #02-2666 for any fee payment deficiencies associated with this case. If the Examiner finds that this case is in any way not in proper form for allowance, the applicants request that the Examiner contact the applicants' representative at (310) 252-7621.

Respectfully submitted,

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